REMARKS

Claims 1-10 are all the claims pending in the application.

Drawings:

The Examiner has objected to the drawings. Applicants have submitted herewith corrected replacement sheets of FIGS. 3, 4, 9, 10, 13, 15 and 16.

Claim Objections:

The Examiner has suggested minor amendments that would make the present claims more clear. Applicants have amended the claims in accordance with the Examiner's suggestions.

Claim Rejections:

A. 35 U.S.C. § 102(e)

Claims 2 and 3 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Barrenscheen et al. (U.S. Patent Publication No. 2003/0084226 A1). Barrenscheen et al. relates to a data transmission device that forwards data that have been received from a first device, intended for a second device, to the second device.

Barrenscheen et al states that its data transmission device is distinguished in that it has connections for connecting at least two data buses and can output data received by a first data bus either onto the same data bus or onto another data bus immediately or later. Therefore, the data transmission device can be used selectively, alternately or simultaneously as a DMA controller and a bus bridge (see Abstract).

The Examiner generally alleges that the synchronous bus is shown in Figures 2A and 2B as BUS1, and that the asynchronous bus is shown as BUS2. The Examiner alleges that BUS2 is

an asynchronous bus since is not synchronized with the processor Module BU11. Applicants respectfully traverse this rejection.

First, there is no indication that the bus lines are synchronous or asynchronous, let alone BUS1 being synchronous and BUS2 being asynchronous. Barrenscheen et al. is silent with respect to this feature. Further, Figure 2B teaches against the Examiner's suggestion that BUS2 is an asynchronous bus since is not synchronized with the processor Module BU11. In Figure 2, data is sent from Bu11 to BU23. Finally, there is no suggestion of the particular first through fourth data that is transferred as in the present invention. Rather, Barrenscheen et al. teaches only general transfer techniques. Accordingly, Applicants respectfully submit that claims 2 and 3 distinguish from the cited art.

B. 35 U.S.C. § 103(a)

Claims 4-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki et al. (JP 2000-92365) in view of Barrenscheen et al. Like above, in this rejection, the Examiner uses Barrenscheen et al. as disclosing the claimed synchronous and asynchronous buses. Accordingly, claims 4-6 are allowable for the same reasons discussed above.

Claims 7-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen et al, and further in view of Sodos. These claims are allowable at least based on their dependency on claim 4, the deficiencies thereof not made up for by Sodos. Further, Sodo does not disclose whether its internal and external buses are synchronous and asynchronous.

Claims 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Masayuki in view of Barrenscheen et al, and further in view of Luo et al. (U.S. Patent No. 6,265,885). Applicants respectfully submit that claim 10 is allowable for similar reasons as claim 4.

C. 35 U.S.C. § 102(b)

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Bourke et al. (U.S. Patent No. 5,509,124). Bourke et al. relates to a data processing system where an input/output bus unit (IOBU) is connected to one end of an input output interface controller (IOIC) via an asynchronous bus. The other end of the IOIC is connected to a storage controller (SC) and an input output interface unit (IOIU) via a synchronous bus.

Solely to advance prosecution of exemplary embodiments of the invention, Applicants have amended claim 1 to further define that "the multiplexer receives first data from the processor and transfers the received first data to the first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor."

The Examiner alleges that the "multiplexer in claim 1 corresponds to the "adapter interface" in Bourke et al. Referring to paragraph [54] of the present specification, the multiplexer 321 receives the first data from processor 31 and transfers the received first data to the first memory through the synchronous data bus, or receives the second data from the first memory through the synchronous data bus and transfers the received second data to the processor 31. Also, the multiplexer 321 receives third data from the processor 31 and transfers

the data to the buffer 322, or receives the fourth data from the buffer 322 and transfers the data to the processor 31.

In Bourke et al., there is no disclosure that the adaptive interface performs these described operations.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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AMENDMENTS TO THE DRAWINGS

Applicants submit herewith corrected replacement sheets of FIGS. 3, 4, 9, 10, 13, 15 and 16.